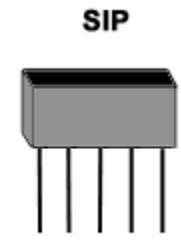
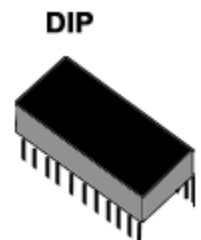




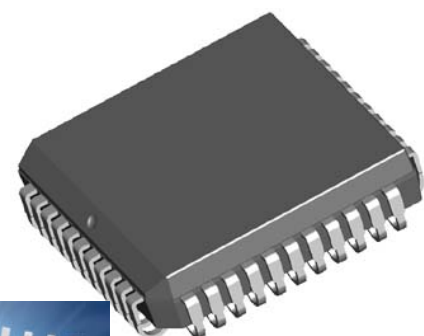
# Hardware Fundamentals

## Simon Chapter 2

# Terminology



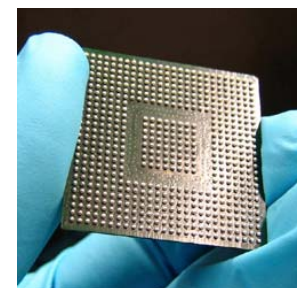
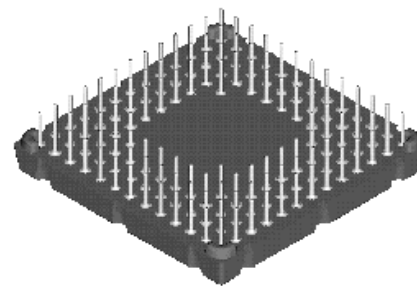
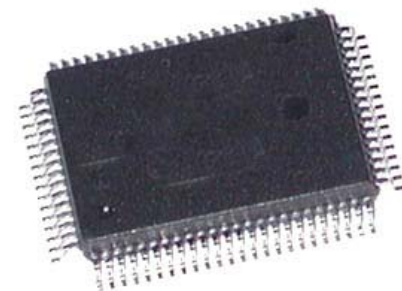
<http://www.computerhope.com>



- Chips, pins, circuit boards

- Packages

- DIP: Dual In-Line Package
- PLCC: Plastic Leaded/Leadless Chip Carrier
- TSOP: Thin Small Outline Package
- PQFP: Plastic Quad Flat Pack
- BGA: Ball Grid Array
- PGA: Pin Grid Array





# Embedded Circuit Boards



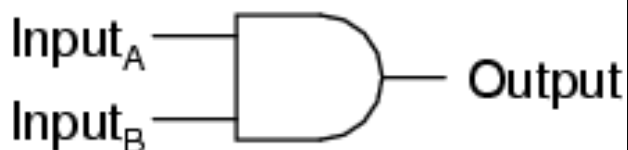
Sparkfun, TI eZ430

# Terminology

- Ground, Low, sometimes battery terminal (-)
- High, VCC, sometimes battery terminal (+)
  - Actually – within a volt or so of the “rails”
- Assertions (negative vs positive)
- Address lines (A0, A1, A2, etc.)
- Data lines (D0, D1, D2, etc.)
- \* or /
- Inputs and outputs...**driving** the signal
- Bus fight – two outputs driving different ways

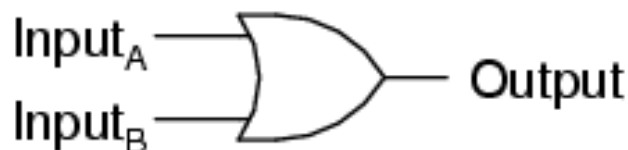
# Gates and Boolean Logic

*2-input AND gate*



A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

*2-input OR gate*



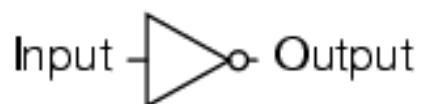
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

*Exclusive-OR gate*



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

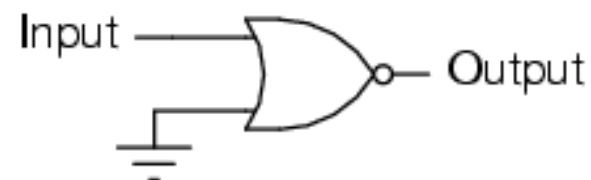
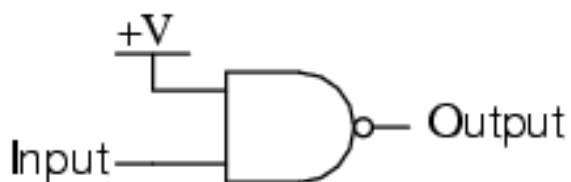
# More Gate Logic



Input	Output
0	1
1	0

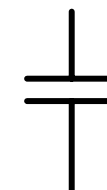
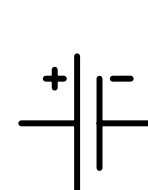
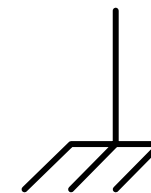


... or ...



(Book example)

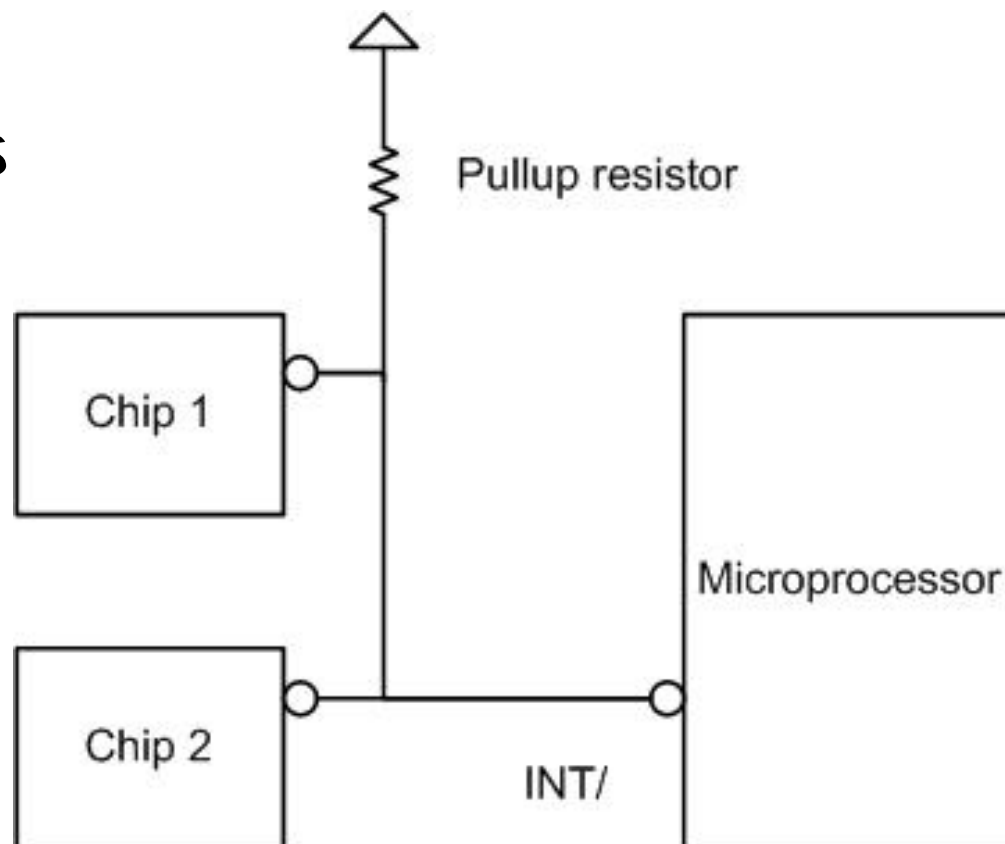
# Other Considerations



- Power surges and decoupling capacitors

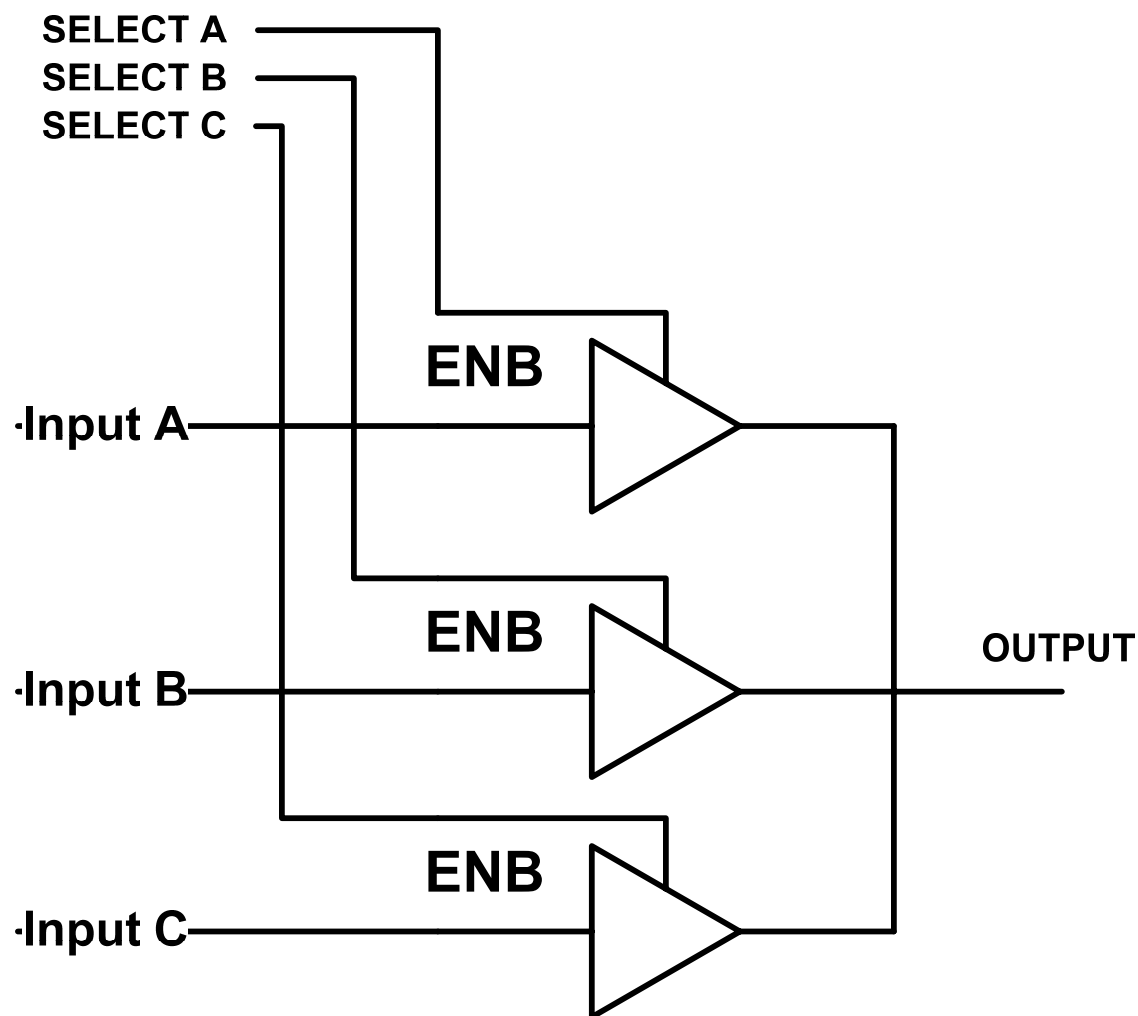
- Open Collector Outputs

- Driving one output with several devices
- Output: low or float
- Pull-up resistor
- No bus fights



# Tri State Devices

- Three states
  - Hi
  - Lo
  - Hi Impedence
- Data Paths
- Overloading



# Timing Diagrams

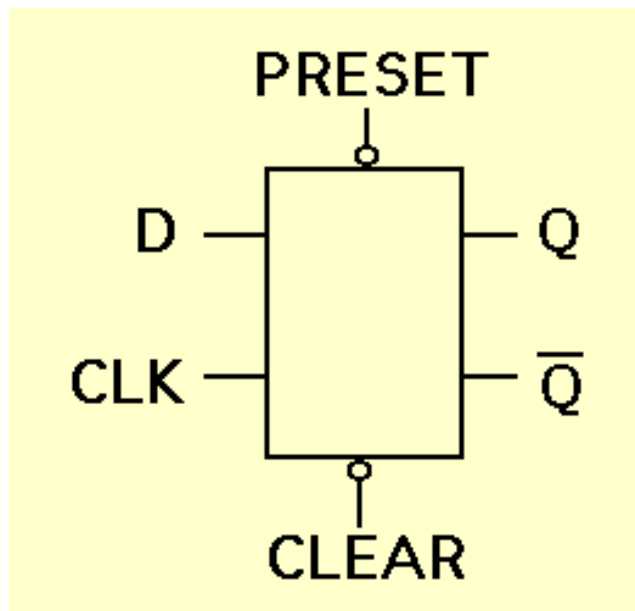
- NAND Gate



NAND

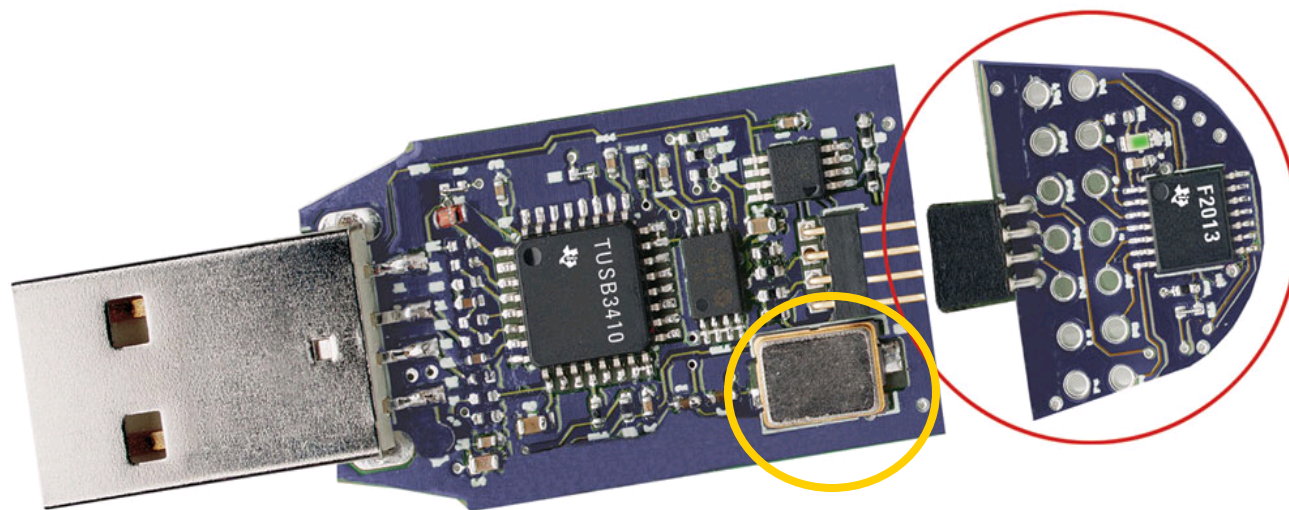
# D Flip Flops: 1-bit Memory

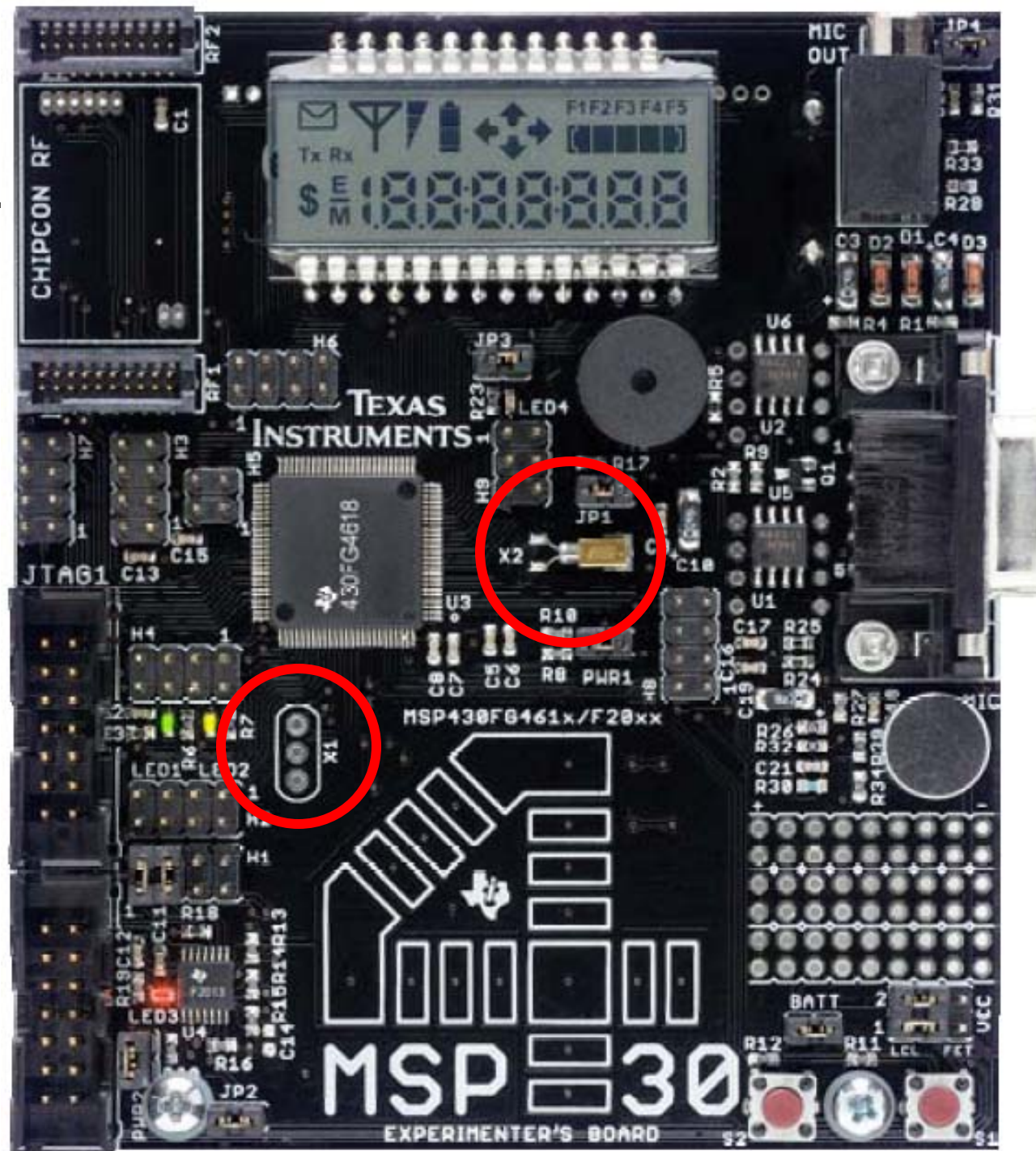
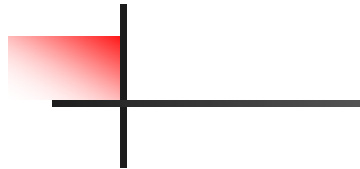
- Operation
  - Rising or Falling Edge Triggered
  - $Q = D$  at clocks rising edge
  - All other times,  $Q$  holds existing value
- Hold time and Setup Time
  - (do plot)



# Clocks

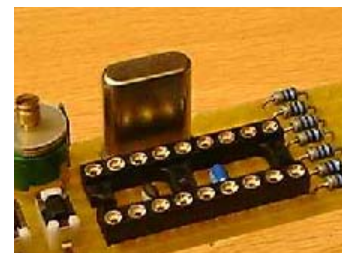
- Oscillators and Crystals
- Timing requirements of components
- Multiple clocks (sleep, Xmit)
- Often integer multiples of data rates





# Schematic Conventions

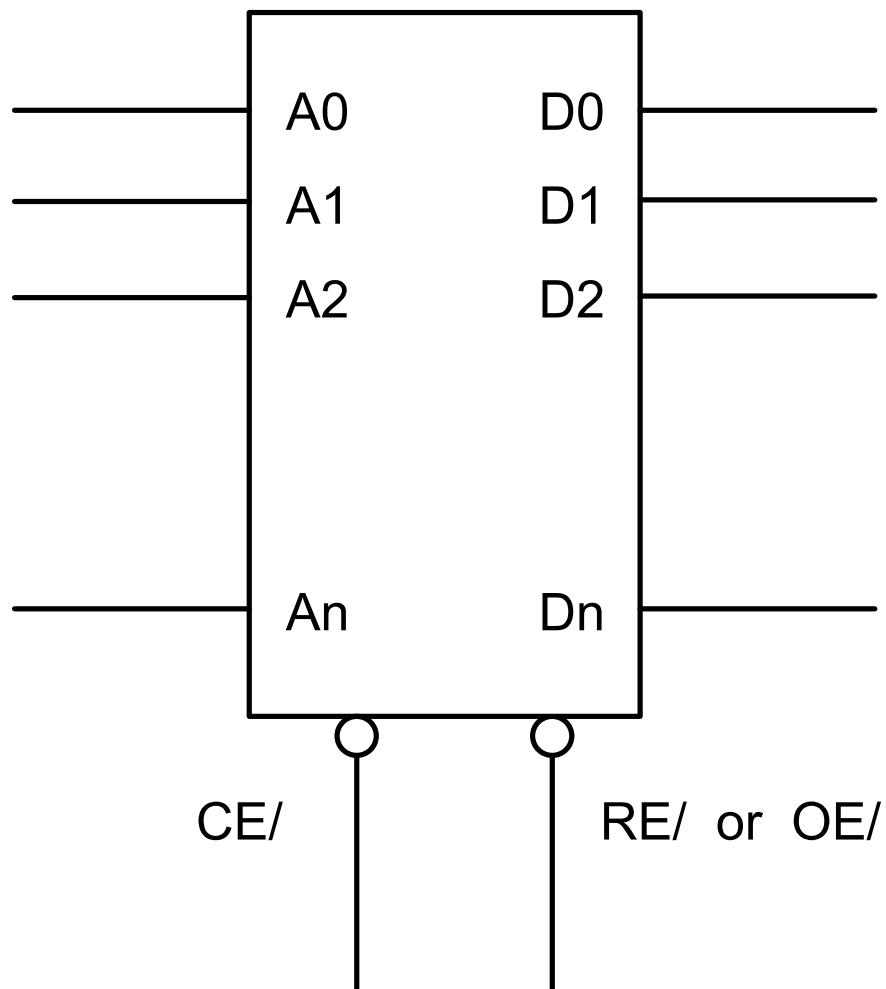
- A15...Address Lines
- D3...Data Lines
- P1, P3...Connectors
- J1, J2...Jumpers (configuratic
- Pins are numbered
- X0, X1 ...cryst
- TP....Test Point
- U7...IC
- R, C, D...discrete componen



# Memory: RAM and ROM

- ROM: Read Only Memory
  - Nonvolatile – data maintained after power off
  - Where programs and some data stored
- ROM Variants
  - PROM: Programmable ROM (used once)
  - EPROM: Erasable Programmable ROM (erased with UV)
  - FLASH: (rewritten by programming)
  - EEPROM: Electronically-erasable ROM (erased electronically, very slow)
- RAM
  - Extremely fast
  - Data lost when power off

# Address and Data Lines



(Timing Diagram)