

IAR Embedded Workbench KickStart

1 CURRENT VERSION: IAR 4.09A/WIN, FET 5.10/WIN

Literature #	slac050q.zip
Executable file name	FET_R510.exe
HIL.dll version	1.2.2.0
MSP430.dll version	2.3.1.0

1.1 KNOWN LIMITATIONS

JTAG2

Attach to running target

Description

The "Attach to running target" feature is not working 100% reliably, especially for Spy-Bi-Wire capable devices.

Workaround

None

EEM7

Advanced Trigger of type Register does not work properly for MSP430X architecture

Description

The configuration of an Advanced Trigger of type Register [e.g., to observe the Stack Pointer (SP) register value] does not show the expected behavior in the case where a device with the MSP430X architecture (e.g., MSP430FG461x, MSP430F241x and MSP430F261x) is target of a debug session.

Workaround

None

IDE1

Key bindings are deleted

Description

If this version of the IAR Embedded Workbench (4.09A/WIN) gets installed in the same subdirectory where a previous version (e.g., 3.42A/WIN) is already installed all key bindings [e.g., debug hotkeys F5 (Go), F10 (Step Over), F11 (Step Into)] will be deleted in both versions.

Workaround

Select in main menu Tools -> Options... -> Key Bindings and push the 'Reset All' button in each IAR installation.

CSPY1 ***Integer values of C-type 'long' (32-bit) are displayed incorrectly in Watch window for MSP430X architecture***

Description	This affects 32-bit values which are held in two CPU registers. E.g. a value of 0x00123456 is stored in R14 and R15. The lower word of the the 32-bit value is stored in R14 = 0x3456 and the higher word is stored in R15 = 0x0012. The C-Spy Watch window shows a value of 0x12003456. This is a problem of the Watch window only, the program code will produce the correct results. It is recommended not to change the dedicated 32-bit value via the Watch window as this can cause unpredictable behaviour. This limitation is only valid in the case where a device with the MSP430X architecture is target of a debug session.
Workaround	None

2 PRIOR VERSION: IAR 3.42A/WIN, FET 4.62/WIN

Literature #	slac050p.zip
Executable file name	FET_R463.exe
HIL.dll version	1.2.2.0
MSP430.dll version	2.1.10.1

2.1 KNOWN LIMITATIONS

JTAG2

Attach to running target

Description

The "Attach to running target" feature is not working 100% reliably, especially for Spy-Bi-Wire capable devices.

Workaround

None

EEM6

Emulator Clock Control is not active by default

Description

The "Emulator -> Clock Control" feature is not enabled by default when the C-Spy debugger gets started.

Workaround

Open "Emulator -> Clock Control" dialog box and close it again by clicking on the OK button. Emulation clock control is now activated.

PRIOR VERSION: IAR 3.42A/WIN, FET 4.62/WIN

3 PRIOR VERSION: IAR 3.42A/WIN, FET 4.62/WIN

Literature #	slac050o.zip
Executable file name	FET_R462.exe
HIL.dll version	1.2.2.0
MSP430.dll version	2.1.10.0

3.1 KNOWN LIMITATIONS

DEVICE2

Support for MSP430F11x1A device derivatives Revision J

Description

Silicon revision J of MSP430F11x1A devices is not recognized correctly by the Emulator driver. It is not possible to download and debug program code on this dedicated silicon revision.

Workaround

None

JTAG2

Attach to running target

Description

The "Attach to running target" feature is not working 100% reliably, especially for Spy-Bi-Wire capable devices.

Workaround

None

4 PRIOR VERSION: IAR 3.42A/WIN, FET 4.61/WIN

Literature #	slac050n.zip
Executable file name	FET_R461.exe
HIL.dll version	1.2.2.0
MSP430.dll version	2.1.9.0

4.1 KNOWN LIMITATIONS

HEADERFILES1 *Definitions in generic header files msp430.h and io430.h*

Description

- Both files do not include any definitions for MSP430F161x devices.
- Both files contain wrong definitions for FE, FG, and FW devices (exclusive MSP430FG461x devices).
- The file msp430.h includes io430x22x2.h instead of msp430x22x2.h for MSP430F22x2 devices.

Workaround

Use device-specific header files rather than the generic header files or edit generic header files accordingly.

CONFIGFILES1 *RAM size definition in Ink430f223x.xcl linker command files*

Description

A value of 02FF is specified for RAM segments (DATA16_I, DATA16_N, DATA16_N, CSTACK, HEAP), which corresponds to a RAM size of 256 bytes. Actually, MSP430F223x devices have 512 bytes of RAM, which results in a value of 03FF.

Workaround

Edit linker command files accordingly.

CONFIGFILES2 *RAM size definition in Ink430f23x0.xcl linker command files*

Description

- RAM segments definition in Ink430f2330.xcl should be 05FF instead of 02FF.
- RAM segments definition in Ink430f2350.xcl should be 09FF instead of 03FF.

Workaround

Edit linker command files accordingly.

JTAG1 *JTAG security fuse blowing for MSP430F23x0 devices*

Description

It is not possible to burn the JTAG security fuse of MSP430F23x0 devices.

Workaround

None

JTAG2 *Attach to running target*

Description

The "Attach to running target" feature is not working 100% reliably, especially for Spy-Bi-Wire capable devices.

Workaround

None

PRIOR VERSION: IAR 3.42A/WIN, FET 4.60/WIN

5 PRIOR VERSION: IAR 3.42A/WIN, FET 4.60/WIN

Literature #	slac050m.zip
Executable file name	FET_R460.exe
HIL.dll version	1.2.2.0
MSP430.dll version	2.1.8.1

5.1 KNOWN LIMITATIONS

DEVICE1

Support for MSP430F22x2 device derivatives

Description

MSP430F22x2 devices are recognized by the Emulator driver as the corresponding MSP430F22x4 derivative. This results in an Emulator warning that the "Chosen derivative (MSP430F22x2) and actual hardware (MSP430F22x4) do not match".

Workaround

The Emulator warning can be ignored. MSP430F22x2 and MSP430F22x4 derivatives are identical in terms of memory configuration. No issue will be caused by ignoring the Emulator warning.

6 PRIOR VERSION: IAR 3.41G/WIN, FET 4.53/WIN

Literature #	slac050l.zip
Executable file name	FET_R453.exe
HIL.dll version	1.2.2.0
MSP430.dll version	2.1.8.0

6.1 KNOWN LIMITATIONS

EEM5

Enhanced Emulation Module Advanced Trigger

Description

Changing the Action in the Advanced Trigger dialog sometimes has no effect, especially with triggers of type Register.

Workaround

Disable/enable the according trigger by unchecking/checking the checkbox in the global Breakpoints window.

PRIOR VERSION: IAR 3.41A/WIN, FET 4.52/WIN

7 PRIOR VERSION: IAR 3.41A/WIN, FET 4.52/WIN

Literature #	slac050k.zip
Executable file name	FET_R452.exe
HIL.dll version	1.2.1.0
MSP430.dll version	2.1.7.0

7.1 KNOWN LIMITATIONS

EEM1 *Enhanced Emulation Module Breakpoint Combiner*

Description It is not possible to combine an Advanced Trigger of type Register with any other configured trigger.

Workaround None

EEM2 *Enhanced Emulation Module Sequencer Control*

Description Opening the Sequencer Control window prevents further debugging. The workbench hangs up.

Workaround None

8 PRIOR VERSION: IAR 3.40B/WIN, FET 4.51/WIN

Literature #	slac050j.zip
Executable file name	FET_R451.exe
HIL.dll version	1.2.1.0
MSP430.dll version	2.1.6.0

8.1 KNOWN LIMITATIONS

EEM1 *Enhanced Emulation Module Breakpoint Combiner*

Description It is not possible to combine an Advanced Trigger of type Register with any other configured trigger.

Workaround None

EEM2 *Enhanced Emulation Module Sequencer Control*

Description Opening the Sequencer Control window prevents further debugging. The workbench hangs up.

Workaround None

EEM3 *Enhanced Emulation Module Clock Control*

Description Any changes made in the Clock Control window have no effect and are discarded after clicking the "OK" button.

Workaround None

EEM4 *Breakpoints*

Description Advanced Triggers of type Register where the specified register is any other CPU register than the SP (Stack Pointer) have no effect.

Workaround None

FLASH1 *Debugger Flash Programming*

Description It is not possible to link any code/data into Information Memory segments B, C, and D of MSP430F2xx devices without erasing DCO calibration data in segment A.

Workaround None

9 VERSION MATRIX: KNOWN LIMITATIONS

Literature #	HEADERFILES1	CONFIGFILES1	CONFIGFILES2	JTAG1	JTAG2	DEVICE1	DEVICE2	EEM1	EEM2	EEM3	EEM4	EEM5	EEM6	EEM7	FLASH1	IDE1	CSPY1
slac050q.zip					☐									☐		☐	☐
slac050p.zip			☐		☐								☐				
slac050o.zip			☐		☐		☐						☐				
slac050n.zip	☐	☐	☐	☐	☐		☐						☐				
slac050m.zip					☐	☐	☐						☐				
slac050l.zip					☐		☐					☐					
slac050k.zip					☐		☐	☐	☐								
slac050j.zip					☐		☐	☐	☐	☐	☐				☐		

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