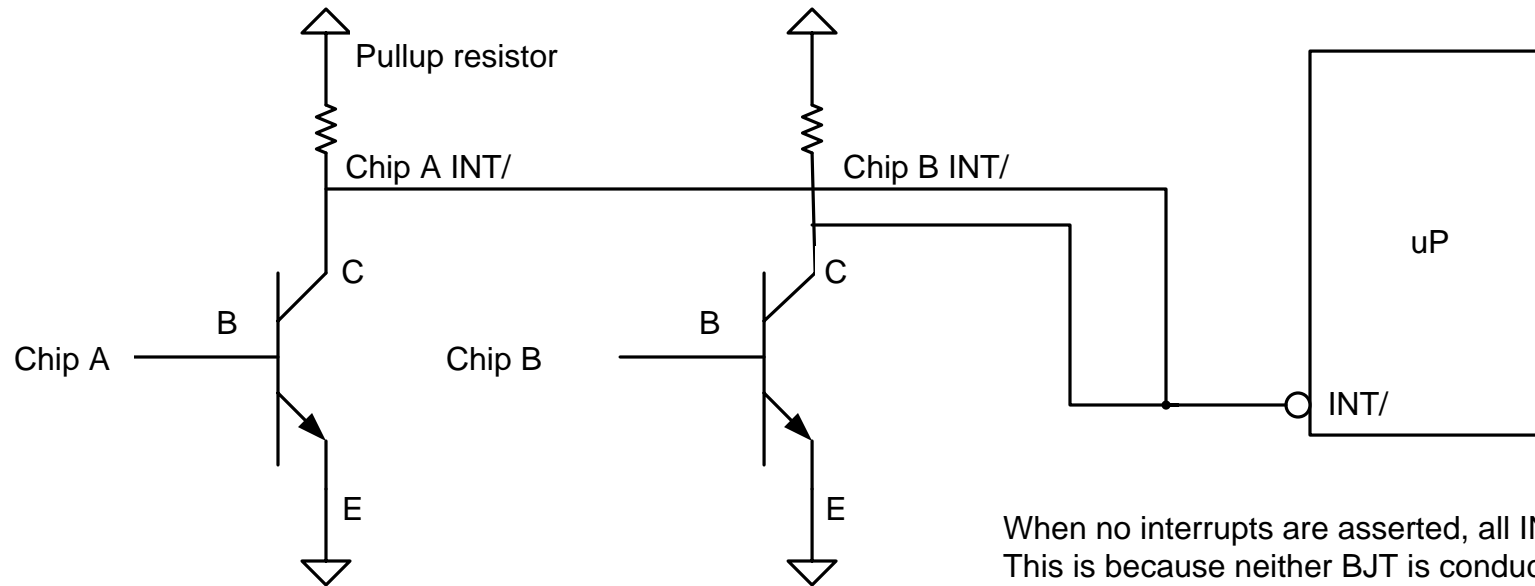


## Here is a sample circuit with open collector “wired-OR” interrupt lines...

Either Chip A or Chip B can interrupt the microprocessor. Both interrupt lines come in on the same IRQ line. Because both are open-collector and each has a pull-up resistor, no “bus fight” will occur.



When no interrupts are asserted, all INT/ lines are HIGH. This is because neither BJT is conducting – no current flows through the BJT or the pullup resistor. That means the voltages at the collectors are HIGH.

### These 4 scenarios can happen...

	Chip A INT/	Chip B INT/	INT/
No one interrupts the uP	HIGH	HIGH	HIGH
Chip A interrupts the uP	LOW	HIGH	LOW
Chip B interrupts the uP	HIGH	LOW	LOW
Both Chip A and B interrupt the uP	LOW	LOW	LOW

Consider the second row, when Chip A asserts its interrupt. The BJT turns ON and conducts, so Chip A INT/ goes LOW. This pin is also connected to the uP INT/ and Chip B INT/. That means the voltage at all those places is LOW.

So Why isn't there a short circuit at Chip B, because Chip B's INT/ line is high?

The critical point is that Chip B is NOT CONDUCTING. It looks like a high impedance open circuit to the rest of the world. So there is NO short circuit to ground through the Chip B BJT. That means point C can be pulled low EXTERNALLY by Chip A, and the current flows through both resistors and then through the Chip A BJT only.